

PROCESSING ARCHITECTURE HAVING PARALLEL ADDITION CAPABILITY

ABSTRACT OF THE DISCLOSURE

According to the invention, a processing core that includes a first source register, a second source register, a multiplexer, a destination register, and an operand processor is disclosed. The first source register includes a plurality of source fields. The second source register includes a number of result field select values and a number of operation fields. The multiplexer is coupled to at least one of the source fields. Included in the destination register is a plurality of result fields. The operand processor and multiplexer operate upon at least one of the source fields.

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